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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,751	12/11/2003	Jonson C. Au	02-6221 1496.00289	8406

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,751	AU, JONSON C.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorst, U.S. Patent No. 6,941,416 B2, in view of Keskar et al., U.S. Patent No. 6,366,989 B1.

Regarding claim 1, Dorst teaches an apparatus comprising:

a memory having a plurality of banks coupled to a memory controller configured to precharge and close all of said plurality of banks prior to a refresh cycle being performed [col. 8, lines 18-28].

Dorst does not teach an interface circuit with a state machine for converting data received at a first data rate to a second data rate.

Keskar teaches an apparatus comprising:

a processor configured to operate at a first data rate response to a first clock signal [Fig. 2, CPU];

an interface circuit [Fig. 2, memory interface 66 a.k.a. "low speed interface"] having a state machine and configured to operate at a second data rate in response to a second clock signal [col. 3, lines 55-59], and convert data received from said processor over a system bus

from said first data rate to said second data rate [col. 1, line 64-67, col. 5, lines 33-42, col. 22, lines 16-20].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Dorst and Keskar by modifying Dorst to implement the low/high speed memory interface of Keskar. Both Dorst and Keskar are directed towards memory interfaces for synchronous dynamic random access memories. The teachings of Keskar would improve the system of Dorst by providing a way to reduce the latency between the CPU and the memories, thus improving overall system performance [Keskar, col. 2, lines 1-14].

Regarding claim 2, it would have been obvious to one of ordinary skill in the art to generate the clocks independently as a matter of design choice.

Regarding claim 3, Keskar teaches that the second clock signal is generated in response to the first clock signal [col. 20, lines 15-19].

Regarding claim 4, Keskar teaches that the state machine is configured to control the conversion between the first and second data rate.

Regarding claim 5, Dorst teaches that the memory controller provides paging to the memory [col. 8, lines 3-4].

Regarding claim 6, Keskar teaches a processor comprising a CPU and a bus interface unit, wherein the CPU communicates through the bus interface unit [Fig. 1, CPU/BIU].

Regarding claim 7, Keskar teaches a bus interface wherein the state machine is configured to communicate with the system bus through the bus interface [Fig. 2, BIU and memory interface].

Regarding claim 9, Dorst teaches that the memory controller is configured to minimize access requests to the memory. The paging scheme of Dorst allows an SDRAM transaction without first having to activate the row based on a previous transfer [col. 8, lines 6-9].

Regarding claims 10 and 11, Keskar/Dorst teaches the apparatus of claim 1. Keskar/Dorst also teaches the method implemented by the claimed apparatus apparatus, and the apparatus with means to achieve the functionality of the claimed apparatus.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorst/Keskar as applied to claims 1-11 above, and further in view of Ghaffari, U.S. Patent No. 7,130,932 B1.

Regarding claim 12, Keskar/Dorst does not teach a DMA engine.

Ghaffari teaches a DMA engine that waits until the system is ready for a DMA transaction [col. 10, lines 23-39].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Keskar/Dorst with Ghaffari by implementing the DMA engine of Ghaffari in the system of Keskar/Dorst. DMA provides the advantage of being able to transfer data from memory to other devices without processor involvement, thus freeing host resources for other uses [Ghaffari, col. 2, lines 5-14].

Claims 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keskar/Dorst/Ghaffari as applied to claim 12 above, and further in view of Tanaka et al., U.S. Patent No 6,470,376 B1.

Regarding claim 13, Keskar/Dorst/Ghaffari does not teach a status register with completion bit for indicating readiness of the DMA operation.

Tanaka teaches a DMA status register with bits for providing a ready/completion status for a DMA operation [col. 25, lines 39-44].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Keskar/Dorst/Ghaffar and Tanaka by implementing the DMA status register as taught by

Tanaka. Although Keskar/Dorst/Ghaffari generally teaches waiting for a DMA ready state, none of the disclosures teach a specific implementation for how such a ready state would be verified. The teachings of Tanaka would improve the combination of Keskar/Dorst/Ghaffari by providing this missing element.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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